ABSTRACT

In one embodiment, an array of content addressable memory (CAM) cells include a first plurality of CAM cells and a second plurality of CAM cells. The second plurality of CAM cells has a width sufficient to address a height of the array. A first plurality of CAM drivers are coupled to the array to drive the first plurality of CAM cells. The first plurality of CAM drivers prevent the first plurality of CAM cells from participating in a match when the array is in a test mode.